A 2-5GHz 100W CW MMIC Limiter using a Novel Input Topology

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A CW 100W MMIC limiter covering 2-5GHz band is presented using TriQuint's 2MI GaAs VPIN process. The new architecture uses a binary power splitter topology to distribute the input power equally to all the input anti-parallel diodes, resulting in higher input power handling capability. The limiter is able to withstand more than 100W of input power with flat leakage less than 16 dBm. The insertion loss is less than 0.5 dB. The input and output return loss is greater than 15 dB. Performance degradation was negligible after a 1 hour test with 100W CW input power.

***Index Terms* — VPIN, Limiter, High Power, MMIC, GaAs, PIN diode**

I. Introduction

With the advent of very high power amplifiers in both HV GaAs and GaN technologies, the industry now needs to improve receiver front end protection circuitry to handle the increased power, pulse widths, and duty cycles that current HPA technologies enable and future systems will require.

GaAs VPIN hybrid limiters have been used to protect LNAs from high incident power for decades [1]. PIN diodes are the preferred choice because they have low insertion loss, low spike leakage, and require no DC power. The existing MMIC VPIN limiters' input power handling capability has been limited to approximately 10W CW before burnout [2, 3].

In this paper, we present a MMIC solution that can handle CW input powers greater than 100W from 2-5 GHz. This new MMIC limiter architecture uses a binary power splitter topology at the limiter's input section to uniformly distribute the input power between the anti-parallel diode pairs. This topology optimally uses all diodes to increase the limiter power handling capability.

II. Basic Limiter Design Considerations

We begin our limiter design discussion from a top down approach. Figure 1-(a) shows the limiter simplified equivalent circuit. The PIN diode is modeled as a parallel RC. The VPIN diodes turn-on when Pin ≥ 13dB. When the limiter is on, R_{diode} << X_{Cdiode} and C_{diode} can be ignored.

Some GaAs LNAs have a 15dB IRL; therefore, we will use $Z_0 = Z_L = 50\Omega$. For an input power (P_{in}) = 100W, equations (1-3) calculate the reflected power ($P_{reflected}$), the limiter dissipated power (P_{diss}), and the delivered power (P_{out}) as functions of R_{diode} for the limiter shown in figure 1-(a). Fig. 1-(b) graphs the calculated powers:

$$P_{out}(W) = 4\left(\frac{R_{diode}}{2R_{diode} + Z_0}\right)^2 P_{in}(W) \quad (1)$$

$$P_{diss}(W) = \left(\frac{1}{2R_{diode} + Z_0}\right)^2 (4 * Z_o * R_{diode}) P_{in}(W) \quad (2)$$

$$P_{reflected}(W) = \left(\frac{Z_o}{2R_{diode} + Z_0}\right)^2 P_{in}(W) \quad (3)$$

If the limiter P_{out} = 20dBm, then Figure 1-(b) shows the following:

R_{diode}: 0.813Ω
$P_{reflected}$: 93.8W
P_{diss}: 6.1W

The VPIN must dissipate 6.1W. To reduce the diode dissipated power, a larger perimeter VPIN with a smaller R_{diode} value must be used to reflect more power. This will result in P_{out} < 20 dBm; however, increasing the VPIN area increases C_{diode} resulting in higher insertion loss or reduction in bandwidth or both.

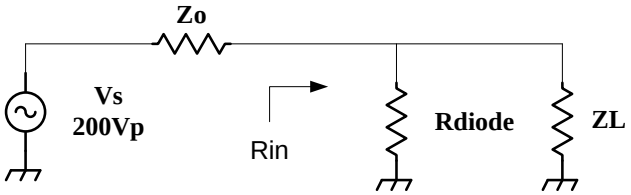

Fig. 1-(a) Equivalent circuit diagram of the limiter circuit

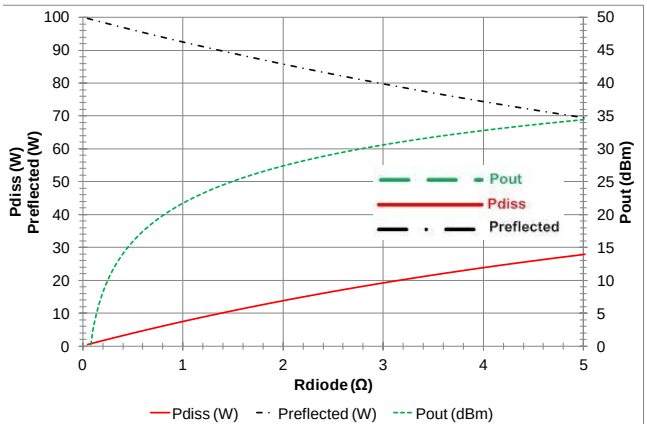

Fig. 1-(b) P_{out}, P_{diss}, & $P_{reflected}$ vs. R_{diode}; P_{in}=100W; (Equations 1-3)

A common technique high power limiter designers [2, 3] use is to add multiple anti-parallel diodes in the input section to reflect more power in order not to exceed the diode's dissipated power limit. Figure 2 shows a typical limiter input topology. The anti-parallel diode sections' physical separation can result in significant electrical length, which should be minimized for optimum limiter operation.

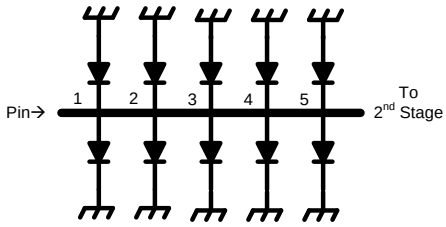

Fig. 2: Conventional limiter diode input string topology

This topology's major limitation is that the first anti-parallel diode pair is prone to burnout before the others because the first anti-parallel diode pair receives more RF power than the remaining pairs in the string. As a result, the current and dissipated power is greatest in the first anti-parallel diode pair. The rear anti-parallel diodes contribution to the large signal limiting action is minimal, while their parasitic capacitance negatively impacts the small signal bandwidth performance.

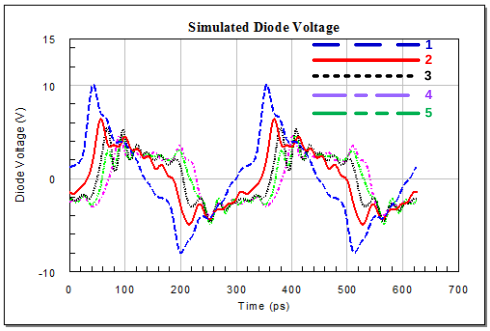

Fig. 3-(a) Simulated diode junction voltage; Pin=100W; freq=3.2GHz

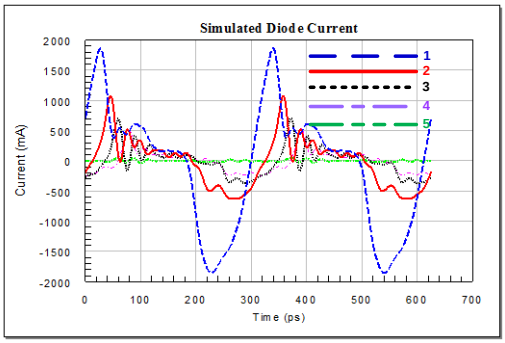

Fig. 3-(b) Simulated diode current; Pin=100W; freq=3.2GHz

Figure 3-(a) shows the simulated voltage across each anti-parallel diode pair. The simulations used a custom fit Caverly PIN diode model. A brief model description will be given in the next section. The simulation shows the voltage across each diode pair monotonically decreases from the front to the back of the diode string.

The diode resistance is inversely proportional to the voltage across the diode. Each anti-parallel diode pair's resistance is not equal because each junction voltage is not uniform; therefore, $R_{diode,1} < R_{diode,2} <\ldots< R_{diode,n}$. Because of these two effects, a significant current non-uniformity exists between the anti-parallel diode sections, as shown by the simulated current waveforms in Figure 3-(b).

The diode I^2R loss is a significant failure mechanism because the current through the first anti-parallel section is much larger than other diode pairs in the stack, as shown in figure 3-(b). As a result, this topology is prone to burnout at lower input power levels.

Figure 4 shows our new input limiter architecture. This architecture approach uses a binary power splitting technique that equally distributes the incident power to all diode pairs. As a result, all the anti-parallel diodes participate equally in the limiting action and dissipate the same power. Thus, the limiter can handle higher input power before burnout occurs. This is a major advantage over the conventional limiter diode input string topology.

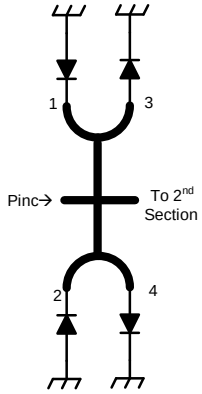

Fig. 4: New limiter input topology using binary splitters

Figure 5-(a) shows that the binary splitter topology results in better voltage uniformity at each anti-parallel section. Because the voltage is uniform at each junction, each diode has the same voltage and current; therefore, all the diode resistances are equal. This lowers the total limiter input resistance, increasing the reflected power, and lowering each diode's dissipated power. Hence, the total dissipated power is equally distributed to all the diode pairs. Figure 5-(b) shows the simulated current in each anti-parallel section is uniform and lower.

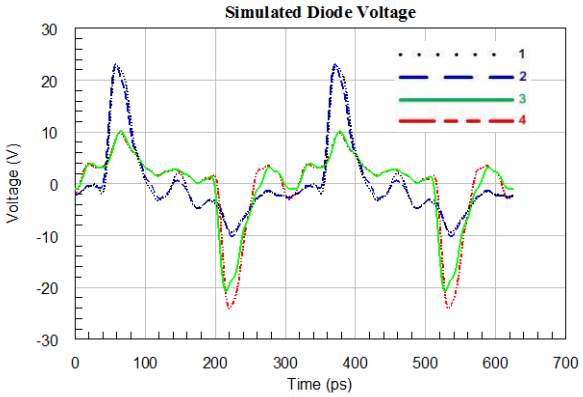

Fig. 5-(a): Simulated diode junction voltage; Pin=100W; freq=3.2GHz

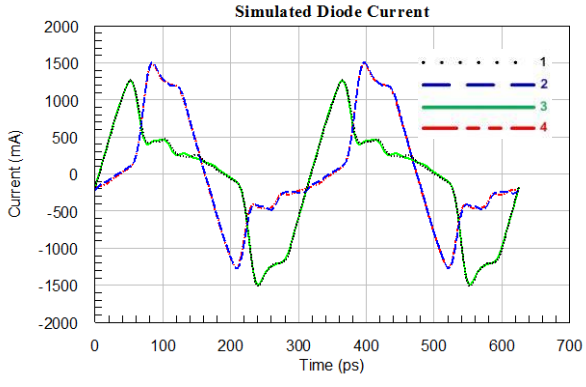

Fig. 5-(b): Simulated diode current; Pin=100W; freq=3.2GHz

III. VPIN MODEL

All circuit simulations used a custom fit AWR Caverly PINDRC non-linear diode model. The off state small signal diode capacitance and resistance were determined from measured s-parameters for diodes widths from 15µm to 100µm. The derived C_{off} area dependence allowed us to determine C_{off} for diode widths from 100µm to 200µm.

We adjusted the PINDRC diode model's R_{lim} parameter to match the simulated Pin vs. Pout to the measured data for diodes widths from 15µm to 100µm. AWR APLAC Harmonic Balance was used for all non-linear simulations. Burnout power testing was done on diodes widths from 15µm to 100µm. The derived burnout-power perimeter dependence allowed us to determine burnout power for diode widths from 100µm to 200µm.

The DC Is and ideality factor were determined from measured DC IV data for diode widths from 15µm to 100µm.

Although the PINDRC model uses several intrinsic Si diode parameters, our non-linear model demonstrated good agreement with measured P_{out} vs. P_{in} at 3.2GHz, and s-parameters from 0.5 to 25.5 GHz.

IV. LIMITER DESIGN

In the previous sections we discussed the new binary splitter input topology's analysis and design extensively. We will discuss the limiter design in two parts: large and small signal performance.

Figure 6 shows the limiter schematic. The input stage has two binary power splitters. Each binary power splitter has three series connected diodes arranged in an anti-parallel configuration. The series-connected configuration increases the input section's turn-on to higher input power levels, approximately 6dB per each anti-parallel pair serially added. The input stage capacitance is about (4/3)* $C_{single,diode}$. Similarly, the input stage resistance is about (¾) * $R_{single,diode}$.

The middle section uses a single anti-parallel pair whose capacitance is optimized to achieve the desired the small signal response. The last stage's main function is to maintain a flat output power.

At lower input power levels, the limiting action occurs in the middle and last diode sections. These sections must have enough power handling capability to withstand and reflect the input power until the input stage diodes turn on.

A high-low pass topology was used to achieve the best small signal performance in-band IL, IRL, and ORL.

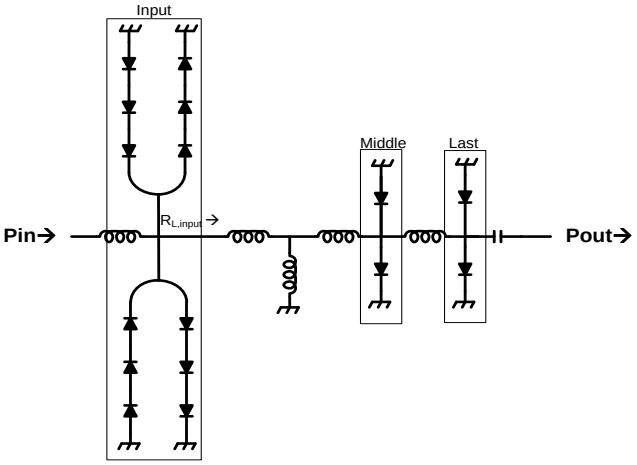

Figure 6 – Basis limiter schematic

V. RESULTS

Figure 7 shows a realized MMIC limiter with the binary power splitting topology using TriQuint's 2MI GaAs VPIN process. TriQuint's 2MI GaAs VPIN process provides excellent high frequency, low parasitic VPIN diodes. The s-parameters were measured on-wafer at TriQuint's RF-Probe testing facility. All CW power measurements and the one hour life test were performed in-fixture in TriQuint's engineering lab.

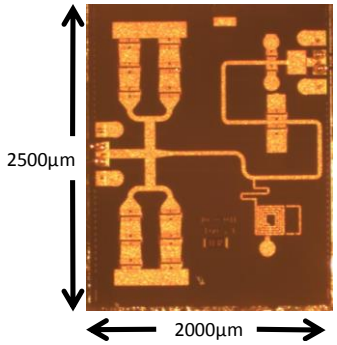

Fig. 7: Fabricated MMIC limiter

Figure 8 shows the RF probe measured s-parameter results for die from one wafer. The IL is less than 0.5dB and the IRL and ORL is greater than 15 dB from 2-5 GHz. Figure 8 also compares the measured s-parameters with the simulated s-parameters.

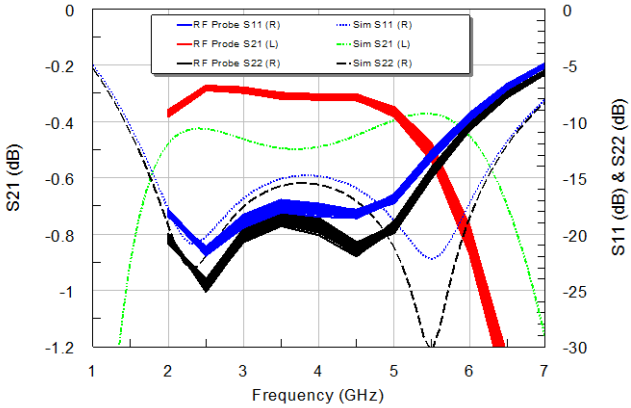

Fig. 8: RF Probe and Simulated IL, IRL, and ORL

The measured BW is about 0.5GHz lower than simulated BW because our C_{off} estimate is a little low. Figure 9 shows the in-fixture P_{out} vs. P_{in} results at 2, 3, and 4 GHz from 10-50dBm. P_{out} is less than 16dBm. The test set is limited to $P_{in} \leq 100W$; therefore, the burnout level could not be determined.

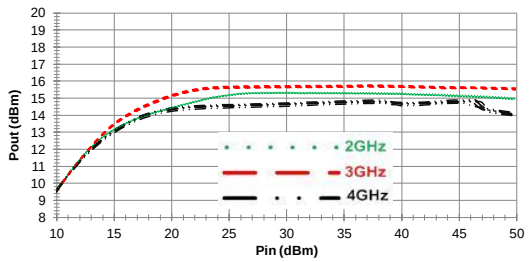

Fig. 9: In-fixture measured CW P_{in} vs. P_{out} at 2, 3, and 4GHz

Figure 10 shows the ΔP_{out} results after applying 100W CW P_{in} for one hour. No significant degradation in performance was observed.

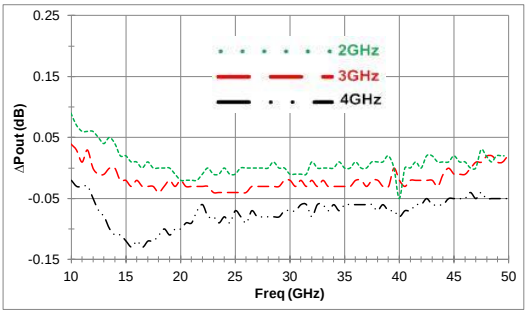

Fig. 10: ΔPout after 100W applied for 1 Hr.

IV. Conclusion

The binary power splitting topology optimally uses all the anti-parallel diodes to increase the limiter's power handling capability. This new input topology's advantage is an equal power distribution across all the diodes. An equal power distribution results in better voltage and current uniformity, lowering the limiter's input resistance. The lower limiter input resistance reflects more power and decreases each diode's dissipated power. Because the total dissipated power is distributed evenly between the diodes, the limiter achieves a higher burnout level.

A 2-5 GHz MMIC high power limiter was fabricated using TriQuint's 2MI VPIN process. Testing the limiter with Pin=100W from 2-5GHz resulted in the following performance:

1. IL < 0.5dB
2. IRL and ORL > 15dB
3. Pout < 16dBm
4. No measurable spike leakage.

Exposing the limiter to 100W CW power for one hour resulted in no significant performance degradation. To our knowledge, this is the highest CW power VPIN MMIC limiter performance recorded. This MMIC limiter can replace the current larger hybrid limiters in Transmit/Receive modules.

References

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